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level Verilog Code of 4-to-1 Multiplexer/Mux and  
Testbench simulation in ModelSim

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Finite State Machines explained  
FPGA Math - Add, Subtract, Multiply, Divide - Signed vs. Unsigned  
Designing a Simple Voting Machine using FPGAs with Verilog HDL and Vivado  
~~FIFO Verilog Code Digital Design \u0026amp; Comp. Arch. Lecture 7b: HW Description Lang. \u0026amp; Verilog (ETH Zürich, Spring 2020) Write, Compile, and Simulate a Verilog model using ModelSim Design of Digital Circuits - Lecture 6: Sequential Logic Design (ETH Zürich, Spring 2019) Simple Combinational Logic Design in Verilog Perl Tutorial ALU Design in Verilog with Testbench | Simulation in Modelsim | Arithmetic Logic Unit~~  
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@ceilingcat Having gone through the blogpost, you

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don't simply compare the MSB. It is a bit more involved than that. There are three conditions for the  $A > B$  case: 1)  $MSB == 0$ , 2) no underflow, and 3) the result is non-zero.

~~How to find MAX or MIN in Verilog coding? Stack Overflow~~

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Decoder v2 - Xilinx 02 dB) but with the complexity of the MAX algorithm If the small reduction in BER performance is acceptable, this provides the best BER Max Log Map Verilog Code Sdocuments2 Verilog code for 2:1 MUX using gate-level modeling For the ...

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available to all. The web page is pretty simple ...

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Fig. 3 and 4 show the BER performances of the Log-Map, the Max-Log-Map, and the modified Max-Log-Map with scaling factor 0.7 after 6 decoding iterations for interleaver lengths 5114 and 1024 respectively. A constant scaling factor (0.7) provides approximately 0.4 dB improvement over the standard Max-Log-Map algorithm at a BER of  $10^{-4}$ .

## ~~The Modified Max Log MAP Turbo Decoding Algorithm by ...~~

This contains BER simulation both Log-MAP and Max-



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Log MAP for a range of Eb/No with graphical representation of BER Vs Eb/No. For any clarifications on this code, Reach me through comment box. Cite As Vinay kumar Reddy (2020). Log ...

~~Log MAP and Max Log MAP File Exchange MATLAB Central~~

By analogy,  $\log(N)$  doesn't get executed by a processor. It calls a bunch of lower-level assembly instructions to do so. Those assembly instructions are part of the  $\log(N)$  library (C, C++, etc.) To be able to synthesize  $\log(N)$  for ASIC/FPGA it requires an instance of a  $\log(N)$  IP core.

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~~Logarithm in Verilog — Stack Overflow~~

The converter analyzes the code of each generator and maps it to equivalent constructs in the target HDL. For Verilog, it will map generators to always blocks, continuous assignments or initial blocks. For VHDL, it will map them to process statements or concurrent signal assignments. The module ports are inferred from signal usage

~~Conversion to Verilog and VHDL — MyHDL 0.11 documentation~~

calculate  $\log_2(n)$  in verilog. I am wondering if  $\log_2(n)$  can be done in verilog as: parameter InputLength = 8; parameter CounterSize =  $\log_2(\text{InputLength})$ ; are not

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acceptable. Thank you in advance, Goanna.  
d\*\*\*@gmail.com 2006-07-05 14:52:38 UTC.  
Permalink. Post by goanna Hi, I would like to parameterize a counter to count an  $n$  bit binary input. Thus the size of the count is at least  $\log_2(n)$  bits ...

~~how to do  $\log_2(n)$  in verilog?~~

Intek provides Verilog HDL design examples as downloadable executable files or displayed as text in your web browser. Select the executable file link to download the file to your hard disk. To use Verilog HDL examples displayed as text in your Intel Quartus Prime software, copy and paste the text from your web browser into the Text Editor. Make sure that the

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file name of the Verilog HDL design ...

## ~~Verilog—Intel~~

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## ~~Creating Verilog HDL Designs for Use with MAX+PLUS II Software~~

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Decoding turbo codes with the max-log-MAP algorithm is a good compromise between performance and complexity. The decoding quality of the max-log-MAP decoder is improved by using a scaling factor ...

~~(PDF) Verilog Implementation of Turbo Encoder and Decoder ...~~

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Further, please see the SystemVerilog-designs in Chapter 10, which provides the better ways for creating the FSM designs as compared to Verilog. Comparison: Mealy and Moore designs ¶

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section{ }label{ } FMS design is known as Moore design if the output of the system depends only on the states (see Fig. 7.1 ); whereas it is known as Mealy design if the output depends on the states and external ...

~~7. Finite state machine — FPGA designs with Verilog and ...~~

expr : Input expression. zeros : Array of pairs of real numbers representing the zeros of the Laplace transform. Each pair consists of a real part and an imaginary part with the r

~~Verilog A Manual: Verilog A Functions — SIMetrix~~

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When looking at Verilog and VHDL code at the same time, the most obvious difference is Verilog does not have library management while VHDL does include design libraries on the top of the code. VHDL libraries contain compiled architectures, entities, packages, and configurations. This feature is very useful when managing large design structures. Examples of packages and configurations in VHDL ...

~~Verilog vs VHDL: Explain by Examples—  
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von Sean Zheng (Guest) 2016-01-01 21:43. Rate this



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post 0 useful not useful: I am a beginner of Verilog. I am trying to build an N-bit-comparator. But I found no information for any generic map. I know in VHDL I can do generic (N: integer:=4); so that I can modify bits when I want to use ...

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