

## Sp601 Hardware User Guide

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The SP601 board enables hardware and software developers to create or evaluate designs targeting the Spartan®-6 XC6SLX16-2CSG324 FPGA. The SP601 provides board features for evaluating the Spartan-6 family that are common to most entry-level development environments.

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Inside every SP601 is a 1.5kW, 2.0kW or 3.0kW flouropolymer coated element, an over temperature cut-out device, a temperature sensor, a water sensor, and a controller circuit board which includes an isolating transformer.

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Preface: About This Guide 8 www.xilinx.com SP605 Hardware User Guide UG526 (v1.9) February 14, 2019 This guide describes the clocking resources available in all Spartan-6 devices, including the DCMs and PLLs. † Spartan-6 FPGA Block RAM Resources User Guide This guide describes the Spartan-6 device block RAM capabilities.

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### **Sp601 Hardware User Guide**

o Hardware User Guide – Detailed description of the SP601 Board features, jumper settings, options and pin location tables. o Reference Design User Guide – Step by Step guide on understanding, implementing, modifying and customizing the SP601 Reference Designs. o Board Design Files – Schematics/Gerbbers/BOM •Cables & Power Supply.

### **Spartan-6 FPGA SP601 Evaluation Kit FAQ**

SP601 Setup. Connect a USB Mini-B Cable to the USB JTAG connector on the SP601 board. – Connect this cable to your PC. Compile MultiBoot Design. Unzip the rdf0006.zip file. Note: Presentation applies to the SP601. Compile MultiBoot Design. At a command prompt, type: cd sp601\_multiboot run\_all\_build\_script.bat.

### **XTP038: SP601 MultiBoot Design - Xilinx**

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CiteSeerX - Document Details (Isaac Councill, Lee Giles, Pradeep Teregowda): Xilinx is disclosing this user guide, manual, release note, and/or specification (the "Documentation") to you solely for use in the development of designs to operate with Xilinx hardware devices.

### **CiteSeerX — SP601 Reference Design User Guide**

SP601 BIST Design Description. Description. – The Built-In System Test (BIST) application uses an EDK MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run. Reference Design IP.

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