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CS250 Tutorial 5
(Version 091210b)

September 12, 2010

Yunsup Lee. In this tutorial you will gain experience using Synopsys Design Compiler (DC) to perform hardware synthesis. A synthesis tool takes an RTL hardware description

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and a standard cell library as input and produces a gate-level netlist as output. The resulting gate-level netlist is a completely structural description with standard cells only at the leaves of the design.

~~RTL to Gates
Synthesis using
Synopsys Design~~

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Execute the unified
physical synthesis
flow. Apply the power

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intent (UPF) Manage
RTL-PG constructs.
Enable Incomplete
UPF support. Apply a
floorplan. Configure
Fusion Compiler to
create a floorplan on-
the-fly. Perform
MCM setup: Define
the corners, modes
and scenarios
required for. analysis
and optimization.

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Design Compiler NXT
technology User

innovations include
fast, highly efficient
optimization engines,
cloud-ready
distributed synthesis,
a new, highly
accurate approach to
RC estimation and
capabilities required
for the process nodes

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5nm and below.

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technologies in Design Compiler NXT and are looking

forward to deploying them on our designs to help meet our ever-

increasing pressure of time-to-market and higher QoR."

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—Synopsys~~

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parameters in the core and set the boundaries and cross dependencies of these parameters.

Users can also easily capture clock information, define the hierarchy of the core, and set constraints of the internal and external ports contained in the core.

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coreBuilder+

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Design Compiler

(Synopsys) Leonardo

(Mentor Graphics)

Front-End Design &

Verification. Create

Behavioral/RTL HDL

Model(s) Simulate to

Verify. Functionality.

Synthesize. Circuit.

Synopsys Design

Compiler. Cadence

RTL Compiler. ...

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Define in file

.synopsys_dc.setup

DC User Guide.

Chapter 4.

Guide

~~Automated Synthesis
from HDL models~~

In this tutorial you will gain experience using Synopsys Design Compiler (DC) to perform hardware synthesis. A synthesis tool takes an RTL

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hardware description
and a standard cell
library as input and
produces a gate-level
netlist as output.

~~RTL to Gates~~

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The Synopsys

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Solutions (SDS) team

brings 3 decades of

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experience and a vast first pass silicon track record built upon Synopsys' technology leadership. SDS works closely with customers to disrupt traditional design process, enabling them to meet and exceed the most stringent requirements, driving

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next generation
subsystem and SoC
innovation beyond
existing architectural
limits.

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this tutorial you will
use Synopsys Design
Compiler to elaborate
the RTL for our

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example greatest
common divisor
(GCD) circuit, set
optimization
constraints,
synthesize the design
to gates, and prepare
various area ... 4
Manual Design
Compiler Build
Process ... # to verify
that latches and flip-
flops are not being
accidentally inferred.

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~~Rtl Compiler User
Guide For Flip Flop~~

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and runs an extensive suite of internal compiler verification and validation tests, and runs C and C++ validation suites from Plum Hall, Inc. and Perennial, Inc. prior to every product release.

The DesignWare ARC

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MetaWare C/C++
Debugger fully
supports the rich set
of ARC configuration
options and
extensions.

~~DesignWare ARC
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Development Toolkit~~
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Synopsys, Inc.
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Software and IP used in the design, verification and manufacture of electronic components and systems, today announced it intends to incorporate on-chip variation (OCV) extensions in its open-source Liberty™ library format, the de-facto modeling standard for

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integrated circuit (IC)
implementation and
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